IN THE CLAIMS:

Claim 1 (previously presented). A method of exercising components on integrated circuits; comprising the steps of:

providing a plurality of integrated circuits each having an optically sensitive device and a component wherein said optically sensitive device is electrically connected to said component;

simultaneously connecting each of the plurality of integrated circuits to an electrical source; and

optically stimulating as follows:

providing a probe card having a plurality of apertures therein;

aligning said apertures with ones of said optically sensitive devices;

providing a source light beam through said apertures to optically stimulate said optically sensitive devices; and,

simultaneously optically stimulating said optically sensitive devices so as to allow current to flow through said optically sensitive devices from said electrical source to said components so as to exercise said components.

Claim 2 (previously presented). The method of claim 1 wherein said electrical source is a power source and wherein said current flow is a positive current flow to said components.

Claim 3 (previously presented). The method of claim 1 wherein said electrical source is an electrical ground and wherein said current flow is a negative current flow to said components.

Claim 4 (previously presented). The method of claim 1 wherein said optically sensitive devices are diodes.

Claim 5 canceled.

Claim 6 (previously presented). The method of claim 1 wherein the step of optically stimulating said optically sensitive devices comprises providing a filter mask, and activating said filter mask for a predetermined time period to allow passage of a light beam through said filter mask to optically stimulate said optically sensitive devices for said predetermined time period.

Claim 7 (previously presented). The method of claim 1 wherein the step of providing a plurality of integrated circuits comprises providing a wafer having said plurality of integrated circuits thereon.

Claim 8 (previously presented). The method of claim 1 wherein the step of optically stimulating said optically sensitive devices comprises providing a fiber optic bundle having individual strands therein, aligning selected ones of said individual strands with ones of said optically sensitive devices, and providing a light beam through said selected ones of said individual strands to optically stimulate ones of said. optically sensitive devices.

Claim 9 (previously presented). The method of claim 1 wherein the step of connecting the integrated circuits to an electrical source comprises providing a probe card having an electrical lead connected at a first end to said electrical source and connected at a second end to a plurality of electrically conductive bumps, and connecting said electrically conductive bumps to ones of said integrated circuits.

Claim 10 (previously presented). The method of claim 9 wherein said probe card includes multiple layers therein including a power source layer connected to said electrical lead, an insulation layer and a ground layer positioned opposite said insulation layer from said power source layer and connected to an electrical ground, and wherein said probe card further includes a plurality of apertures that each extend through said multiple layers so as to allow the passage of light through said probe card to said integrated circuits.

Claim 11 (previously presented). A device for exercising components on a plurality of integrated circuits, comprising:

a probe card including:

a power source connection electrically connected to an outside power source and electrically connected to a power source contact pad on each of a plurality of integrated circuits during exercising of the integrated circuits;

a ground connection electrically connected to an outside electrical ground and electrically connected to a ground contact pad on

each of the plurality of integrated circuits dining exercising of the integrated circuits;

a plurality of apertures that extend through said probe card and that are aligned with an optically sensitive device on each of said integrated circuits during exercising of the integrated circuits; and

a light source that provides a bean of light through said apertures so as to optically stimulate said optically sensitive devices to exercise said integrated circuits.

Claim 12 (previously presented). The device of claim 11 further comprising a filter mask that allows passage of said beam of light through said apertures for a predetermined time period to optically stimulate said optically sensitive devices for said predetermined time period.

Claim 13 (previously presented). The device of claim 11 further comprising a fiber optic bundle having individual strands therein, wherein selected ones of said individual strands are aligned with said apertures, and, wherein said selected ones of said individual strands transmit said beam of light from said light source to said apertures.

Claim 14 (previously presented). The device of claim 11 wherein said light source is chosen from the group consisting of a light bulb, multiple light bulbs, a laser, multiple lasers, and a liquid crystal display panel.

Claim 15 (previously presented). The device of claim 11 further comprising a burn-in chamber containing said probe card and said light source, and further comprising a light control signal for controlling said light source, a multi-filter mask for filtering said light, a light channel controller for controlling said light from said light source, a fiber optic block for transmitting said light from said light source to said probe card, a heating device for heating said integrated circuits, and a temperature control device for controlling said heating device.

Claim 16 (previously presented). The device of claim 15 wherein said burn-in chamber further comprises a parabolic reflector for directing said light to said probe card, said light control signal comprises a liquid crystal display panel, said multi-filter mask comprises at least one wavelength filter, said light channel controller comprises a computer, said fiber optic block comprises a fiber optic bundle, said heating device comprises heating coils, and said temperature control device comprises an anodized aluminum plate connected to a thermostat.

Claim 17 (previously presented). A device for exercising a component on an integrated circuit, comprising:

a probe card including:

a power source connection electrically connected to an outside power source and electrically connected to a power source contact pad on the integrated circuit during exercising of the integrated circuit;

a ground connection electrically connected to an outside electrical ground and electrically connected to a ground contact pad on the integrated circuit during exercising of the integrated circuit;

an aperture that extends through said probe card and that is aligned with an optically sensitive device on said integrated circuit during exercising of the integrated circuit; and

a light source that provides a beam of light through said aperture so as to optically stimulate said optically sensitive device to exercise said integrated circuit;

wherein said probe card extends across a diameter of a wafer containing multiple integrated circuits thereon and wherein said power source connection of the probe card comprises a power source layer that is connected to a power source contact pad on each of the integrated circuits during exercising of the integrated circuits, wherein said ground connection of the probe card comprises a ground layer that is connected to a ground contact pad on each of the integrated circuits during exercising of the integrated circuits, and wherein said probe card includes multiple apertures that extend through said probe card and are aligned with corresponding ones of an optically sensitive device of each of the integrated circuits during exercising of the integrated circuits.

Claim 18 (previously presented). A method of exercising components on a wafer of integrated circuit dies, the method comprising:

supplying a wafer including a plurality of integrated circuit dies, each die having an electrostatic discharge (ESD) protection circuit, including a pair of diodes connected between power and ground, electrically connected to a component;

simultaneously connecting each of the die to an electrical source;

optically stimulating the activated ESD protection circuits of each die; and,

supplying electrical test signals to the die components in response to the optical stimulation.

Claim 19 (previously presented). A device for exercising components on a wafer including a plurality of integrated circuit dies, the device comprising:

a probe card including:

a power source connection for each die;

a ground connection for each die;

at least one aperture for each die, extending through the probe card; and,

a light source supplying a beam of light to each probe card aperture.

Claim 20 (currently amended). A method for testing an integrated circuit die using a light source, the method comprising:

forming an integrated circuit die including a component and an optical region with an electrostatic discharge (ESD) protection circuit including a pair of diodes connected between power and ground;

physically connecting a power and ground connection to each die;

selectively activating the optical region;

introducing an optical test signal to the optical region;

converting the optical test signal to an electrical test current as follows:

introducing the optical signal to the ESD circuit diodes; and

generating a current through the diodes in response to the optical signal stimulus;

introducing the electrical test current to the component; and,

electrically testing the component in response to the electrical test signal.

Claim 21 (previously presented). The method of claim 20 wherein introducing an optical test signal to the optical region includes introducing the optical test signal to a first optical region;

wherein electrically testing the component in response to the electrical test signal includes:

the component generating an electrical command signal;

introducing the electrical command signal to a second optical region; and,

converting the electrical command signal to light, whereby the component is identified as having been tested.

Claim 22-23 canceled

Claim 24 (currently amended). An integrated circuit die, the die comprising:

a component having an input to accept an electrical test signal and an output to supply an electrical command signal; [[and,]]

a selectively activated first optically sensitive device having an interface to accept an optical test signal, the first optically sensitive

device converting the optical test signal to an electrical test supplied at an output connected to the component input.

a physical power connector;

a physical ground connector;

a first switch to selectively enable the power connector; and,

a second switch to selectively enable the ground connector.

Claim 25 (previously presented). The die of claim 24 further comprising:

a second optically sensitive device having an input connected to the component output to accept the electrical command signal, the second optically sensitive device converting the electrical command signal to a light signal emitted at an output.

Claim 26-27 canceled

Claim 28 (currently amended). The die of claim [[26]] 24 wherein the optically sensitive device includes:

a first diode with a cathode connected to power and an anode connected to the component input; and,

a second diode with a cathode connected to the component input and an anode connected to ground.

Claim 29 (previously presented). A method of exercising components on integrated circuits; comprising the steps of:

providing a plurality of integrated circuits each having an optically sensitive device and a component wherein said optically sensitive device is electrically connected to said component;

simultaneously connecting each of the plurality of integrated circuits to an electrical source; and

optically stimulating as follows:

providing a fiber optic bundle having individual strands therein;

aligning selected ones of said individual strands with ones of said optically sensitive devices;

providing a light beam through said selected ones of said individual strands to optically stimulate ones of said. optically sensitive devices; and,

simultaneously optically stimulating said optically sensitive devices so as to allow current to flow through said optically sensitive devices from said electrical source to said components so as to exercise said components.

Claim 30 (previously presented). A method of exercising components on integrated circuits; comprising the steps of:

providing a plurality of integrated circuits each having an optically sensitive device and a component wherein said optically sensitive device is electrically connected to said component;

simultaneously connecting each of the plurality of integrated circuits to an electrical source; and

optically stimulating as follows:

providing a probe card having an electrical lead connected at a first end to said electrical source and connected at a second end to a plurality of electrically conductive bumps;

connecting said electrically conductive bumps to ones of said integrated circuits; and,

simultaneously optically stimulating said optically sensitive devices so as to allow current to flow through said optically sensitive devices from said electrical source to said components so as to exercise said components.

Claim 31 (new). A method for testing an integrated circuit die using a light source, the method comprising:

forming an integrated circuit die including a component and a first optical region;

selectively activating the first optical region;

introducing an optical test signal to the first optical region;

converting the optical test signal to an electrical test current;

introducing the electrical test current to the component; and,

electrically testing the component in response to the electrical test signal as follows:

the component generating an electrical command signal;

introducing the electrical command signal to a second optical region; and,

converting the electrical command signal to light, whereby the component is identified as having been tested.

Claim 32 (new). An integrated circuit die, the die comprising:

a component having an input to accept an electrical test signal and an output to supply an electrical command signal;

a selectively activated first optically sensitive device having an interface to accept an optical test signal, the first optically sensitive device converting the optical test signal to an electrical test supplied at an output connected to the component input; and

a second optically sensitive device having an input connected to the component output to accept the electrical command signal, the second optically sensitive device converting the electrical command signal to a light signal emitted at an output.

Claim 33 (new). An integrated circuit die, the die comprising:

a component having an input to accept an electrical test signal and an output to supply an electrical command signal;

a selectively activated first optically sensitive device having an interface to accept an optical test signal, the first optically sensitive device converting the optical test signal to an electrical test supplied at an output connected to the component input;

a physical power connector;

a physical ground connector;

wherein the optically sensitive device includes:

a first diode with a cathode connected to power and an anode connected to the component input; and,

a second diode with a cathode connected to the component input and an anode connected to ground.